06 EC EE ML

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06EC71

Seventh Semester B.E. Degree Examination, June 2012
Computer Communication Networks

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. With a neat diagram, explain the TCP/IP reference model. **(10 Marks)**

b. Explain in detail, the cable TV network used for data transfer. **(06 Marks)**

c. Calculate the minimum time to download the one million bytes of information using each of the following technologies :
   i) V.32 modem
   ii) V.32 bis modem
   iii) V.90 modem. **(04 Marks)**

2 a. With a neat diagram of piggy backing in Go–back–N ARQ protocol, explain the following :
   i) Frame structure of piggy backing
   ii) Types of events occured in piggybacking
   iii) Advantages of piggybacking. **(10 Marks)**

b. With a neat diagram, explain the different types of high level data link control (HDLC) frames. **(06 Marks)**

c. The following character encoding is used in a data link protocol :
A : 01000111; B : 11100011; FLAG : 01111110; ESC = 111 00000. Show the bit sequence transmitted (in binary) for the four character frame : A B ESC FLAG when each of the following framing methods are used :
   i) Character count
   ii) Flag bytes with byte stuffing
   iii) Starting and ending flag bytes with bit stuffing. **(04 Marks)**

3 a. With a suitable flow diagram, explain CSMA/CD protocol and discuss the frame transmission time. **(08 Marks)**

b. Explain the following controlled access methods :
i) Reservation ii) Polling iii) Token passing. **(08 Marks)**

c. Show that the throughput for pure ALOHA is $S = Ge^{-2G}$ and maximum throughput $S_{max} = 0.184$. **(04 Marks)**

4 a. With a neat diagram, explain 802.3 MAC frame format. **(10 Marks)**

b. Explain the following standard ethernet physical layer implementations.
   i) 10 base 5 : thick ethernet
   ii) 10 base 2 : thin ethernet
   iii) 10 base T : twisted pair ethernet
   iv) 10 base F : fiber ethernet. **(10 Marks)**

PART – B

5 a. Explain the following in brief :
   i) Passive hubs
   ii) Active hubs
   iii) Bridges
   iv) Router
   v) Gateway. **(10 Marks)**

   b. Explain virtual LAN system and how the membership is allocated in the V–LAN system. **(10 Marks)**

6 a. What are the differences between classful and classless addressing? **(05 Marks)**

   b. What is network address translation (NAT)? Explain in brief. **(05 Marks)**

   c. Draw the IPV4 datagram format and explain its field. **(10 Marks)**

7 a. Explain in detail, the distance vector routing algorithm. **(10 Marks)**

   b. Explain three different forwarding techniques. **(10 Marks)**

8 a. Explain in detail, user datagram protocol, UDP. **(10 Marks)**

   b. Describe DNS in the internet. **(10 Marks)**

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06EC73

Seventh Semester B.E. Degree Examination, June 2012

Power Electronics

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Give symbol and characteristic features of the following devices :
i) SCR ii) GTO iii) TRIAC iv) IGBT v) SIT **(10 Marks)**

b. Briefly explain any five types of power electronic circuits. **(10 Marks)**

2 a. What is the need for isolation of gate-drive circuits? Discuss the different methods of providing isolation of gate-drive circuits from power circuit. **(10 Marks)**

b. Discuss the switching limits of power transistors. **(10 Marks)**

3 a. With a neat diagram, explain the two-transistor model of a thyristor. Also, derive an expression for the anode current in terms of transistor parameters α_1 and α_2. **(08 Marks)**

b. What is the need of di/dt and dv/dt protection? Explain how protection is provided. **(04 Marks)**

c. With a neat circuit diagram and waveforms, explain UJT relaxation oscillator. **(08 Marks)**

4 a. With the necessary circuit diagram, waveforms and equations, explain the operation of single-phase full converter with R-L load. **(10 Marks)**

b. Explain single-phase semiconverter with a neat circuit diagram, waveforms and equations. **(10 Marks)**

PART – B

5 a. What is commutation? Explain complementary commutation with relevant circuit diagram and waveforms. **(10 Marks)**

b. For the auxiliary commutation circuit, calculate the values of the commutation capacitor and inductor for the following data:
$V_{d_c} = 30V$, $I_{L(max)} = 15A$, t_{off} of SCR1 = 20 µsec. **(04 Marks)**

c. With a neat circuit diagram and waveforms, explain external pulse commutation. **(06 Marks)**

6 a. With neat diagrams, waveforms and equations, discuss ON-OFF control and phase control of AC voltage controllers. **(12 Marks)**

b. A single-phase full-wave AC voltage controller has a resistive load 20Ω and the input voltage is 100 V (rms), 60 Hz. The delay angles of thyristors T_1 and T_2 are : $\alpha_1 = \alpha_2 = \alpha = \frac{\pi}{2}$.
Determine : i) The rms output voltage ; ii) The input power factor ; iii) The average current of thyristors ; iv) The rms current of thyristors. **(08 Marks)**

7 a. What is chopper? How they are classified? Briefly explain. **(10 Marks)**

b. With a neat circuit diagram and waveforms, explain impulse commutated chopper. **(10 Marks)**

8 a. Explain single-phase half-bridge inverter with R load, with necessary circuit diagram and waveforms. Derive the equation for rms output voltage. **(12 Marks)**

b. Explain the performance parameters of inverters. **(08 Marks)**

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06EC74

Seventh Semester B.E. Degree Examination, June 2012

DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. With a neat block diagram, explain the scheme of a DSP system. **(08 Marks)**

b. With an example, explain the need for the lowpass filter in decimation process. **(04 Marks)**

c. For the FIR filter $y(n) = (x(n) + x(n-1) + x(x-2))/3$. Determine :

i) System function ii) Magnitude and phase response function

iii) Step response iv) Group delay. **(08 Marks)**

2 a. Explain the implementation of 4-bit shift left barrel shifter, with a neat diagram. **(06 Marks)**

b. Suggest a scheme to implement a multiplier to multiply two complex numbers using 4 × 4 Braun multiplier as the building block. **(06 Marks)**

c. Draw a structure to multiply two 4-bit signed numbers A and B. **(08 Marks)**

3 a. Explain the functioning of a barrel shifter in a TMS320C54XX processor. **(06 Marks)**

b. With a block diagram, explain the indirect addressing mode of TMS320C54XX processor using Dual memory operand. **(06 Marks)**

c. Consider that AR3 is selected as the pointer for the circular buffer. The various register contents are BK = 40, AR3 = 2020H, AR0 = 0025H. Find :

i) Start and End address of the buffer

ii) Contents of AR3 after execution of the instruction LD* + AR3 (12H)%

iii) Contents of AR3 after execution of the instruction LD* AR3 – %. **(08 Marks)**

4 a. Describe the operation of the following instructions of TMS320C54XX processors :

i) MPY # AR2 –, *AR4 + 0, B ii) RPT # K

iii) RPTB Pmad iv) MAS *AR3 –, *AR4+, B, A **(08 Marks)**

b. Describe the different stages of pipelining in TMS320C54XX processor. **(06 Marks)**

c. Write an assembly language program of TMS320C4XX processors to compute the sum of three product terms given by the equation $y(n) = h_0x(n) + h_1x(n-1) + h_2x(n-2)$ using MAC instructions. **(06 Marks)**

PART – B

5 a. Determine the value of each of the following numbers represented using the given Q-notation :

i) –0.1958 as a Q_{15} number ii) 136 as a Q_7 number

iii) D0B5H as a Q_{15} number iv) 4400H as a Q_7 number **(04 Marks)**

b. Write an assembly language program for TMS320C54XX processors to implement an FIR filter. **(12 Marks)**

c. Explain the Q-notation to multiply two Q_{15} numbers to produce Q_{15} number result. **(04 Marks)**

6 a. Explain a general DIT-FFT butterfly in-place computation structure. Determine the following for 128-point FFT computation:
   i) Number of butterflies in each stage
   ii) Number of butterflies needed for the entire computation. **(06 Marks)**

b. Explain how scaling prevents overflow condition in the butterfly computation. **(06 Marks)**

c. With the help of implementation structure, explain the 8-point DIT-FFT computation on TMS320C54XX processors. Use scale factor = $\frac{1}{4}$ for all butterflies. **(08 Marks)**

7 a. Design an interface to connect a 64K × 16 flash memory to a TMS320C54XX processor. The processor address bus is $A_0 - A_{15}$. **(06 Marks)**

b. Draw the I/O interface timing diagram for read-write-read sequence of operation and also explain the signals that are involved in an I/O transaction. **(06 Marks)**

c. Interface the TMS320C54XX to a 10 bit ADC (TLC 1550) and an 8-bit DAC (TLC 7524). The sampled signal read from the ADC is to be written to the DAC after adjusting its size. The start of the conversion is to be initiated by the TOUT signal of the timer. **(08 Marks)**

8 a. With the help of neat block diagram, explain PCM 3002 CODEC. **(06 Marks)**

b. With the help of block diagram, explain DSP-based biotelemetry receiver system. **(06 Marks)**

c. Explain with a neat diagram, the operation of the pitch detector. **(08 Marks)**

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06EC762

Seventh Semester B.E. Degree Examination, June 2012
Real Time Systems

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define a real time system. Explain generalized computer control system with hardware and software interface details. **(10 Marks)**

b. Classify real time systems based on time constraint with an example for each and appropriate equations. **(10 Marks)**

2 a. With a neat block diagram, explain Direct Digital Control. **(07 Marks)**

b. Write PID control algorithm. **(03 Marks)**

c. Describe supervisory control with a neat block diagram. **(06 Marks)**

d. Discuss gain scheduled programmed adaptive control. **(04 Marks)**

3 a. Briefly explain the following:
i) Parallel computers ii) Polling iii) DMA **(06 Marks)**

b. Explain analog interface for input and output operation. **(08 Marks)**

c. With a neat block diagram, explain interrupt masking. **(06 Marks)**

4 a. Define CUTLASS. What are the major requirements of CUTLASS? Describe CUTLASS host target configuration. **(10 Marks)**

b. With an example program, Explain interrupts and device handling. **(10 Marks)**

PART – B

5 a. Explain typical structure of a real time operating system (RTOS). **(06 Marks)**

b. What are the basic functions of the task management module? With system commands explain RTOS task state diagram. **(10 Marks)**

c. What do you mean by minimum operating system Kernel? List its functions. **(04 Marks)**

6 a. What is code sharing? How do you overcome code sharing problem? Explain. **(10 Marks)**

b. Write a note on detailed arrangement of IOSS. **(05 Marks)**

c. Explain different mechanisms supported by RTOS for the transfer of data between tasks. **(05 Marks)**

7 a. Discuss preliminary design details of real time system. **(10 Marks)**

b. Define mutual exclusion principle and explain mutual exclusion with a neat flow chart and sample program. **(10 Marks)**

8 a. Write a note on:
i) Yourdon methodology. **(05 Marks)**
ii) Drying oven-context diagram. **(07 Marks)**

b. Differentiate : Ward and Mellor methodology and Hotley and Pirbai methodology. **(05 Marks)**

c. List various real time system development methodologies. **(03 Marks)**

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